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| EXAMINER | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/579,577 | DENG, GUOSHUN | |
| | Examiner | Art Unit | |
| | DENNIS MYINT | 2162 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05/17/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1- 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/13/08, and 10/10/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-13 are pending in this application.

### *Priority*

2. Applicant's claim for foreign priority under 35 U.S.C. 119 (a) is acknowledged based on PCT/CN04/03120.

### *Information Disclosure Statement (IDS)*

3. The information disclosure statements (IDS) filed on 03/13/2008, and 10/10/2006 are in compliance with the provisions of 37 CFR 1.97 and have been considered.

### *Specification*

4. The disclosure is objected to because of the following informalities: the specification recites "diskloses"in lines 3 and 7 of paragraph 0003. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 9, the claim is rejected under 35 U.S.C. 112, second paragraph, because the claim makes use of trademarks to further limit claim 1.

**MPEP 2173.05(u)** states that: "the presence of a Trademark or trade name in a claim is not, per se, improper that Trademarks or Trade Names in a Claim under 35 U.S.C. 112, second paragraph……..If the trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of the 35 U.S.C. 112, second paragraph. Ex parte Simpson, 218 USPQ 1020 (Bd. App. 1982)."

Claim 9 in line 3 recites "Windows" which is a trademark of Microsoft corporation. Claim 9 in lines 4 and 7 recites "UNIX" which is a trademark of The Open Group. Claim 9 lines 4 and 7 recites "LINUX" which a trademark owned by Linus Torvalds.

Therefore, claim 9 is rejected under 35 U.S.C. 112, second paragraph, because the claim makes use of registered trademarks.

### *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Butts et al., (hereinafter "Butts", U.S. Patent Number 5812414) in view of Lavallee et al., (hereinafter "Lavallee", U.S. Patent Number 5267242).

As per claim 1, Butts is directed to a data managing method for a removable storage device having a replaceable memory chip (Butts, Figure 3, logic chips and Figure 38 ; Butts, col. 37 lines 38-44, i.e., *" FIG. 38 shows the USDM architecture. Devices are installed on the user-supplied device installation area, which can be an area of the USDM printed circuit board, a removable daughter card plugged into the USDM, or another such area connected via cable in the manner common in microprocessor emulator instruments";* ) and teaches the limitations:

"1) **determining the memory chip"** ( Butts, col. 38 lines 53-57, i.e., *"Control signals are interconnected by the MA chips"; See also,* Butts, col. 38 lines 58-67, i.e., *"The output enable control signals are generated by special logic connected to the control signals as specified above, which is included by the user in the input design and realized in the Lchips with the rest of the design";* particularly, Butts, col. 39 lines 42-46, i.e., *"For each net connected to the USD(s) on this USDM:* ***If it drives a USD input pin****, issue primitives to this pin's logic chip's netlist file for: An input buffer from the receiving path used for this net, driving the input of an output buffer which drives the terminal block pin used for this USD pin"* ), **and "applying or organizing or establishing or re-establishing a file managing system for the storage medium of said removable storage device"** ( Butts, col. 40 lines 1-8, i.e., *"As described in the section on logic and interconnect chip technology, the configuration bit patterns*

*for each chip are generated by the ERCGA netlist conversion tool. The final stage of the Realizer design conversion system collects the data from the configuration files generated for all chips into a single binary configuration file for the design, which is permanently stored in the host computer"* ); and

"2) **utilizing said file managing system to perform corresponding processing in said memory chip according to an operation instruction from a host system connected to said removable storage device**" ( Butts, col. 40 lines 9-19, i.e. *"Once the chips are configured, the total of all their logic* ***functions*** *and interconnections matches that specified by the input design, and* ***operation*** *of the design* ***can proceed****"* ).

Butts does not explicitly teach the limitation: "determining the use condition of said memory chip".

Lavallee teaches the limitation:

"**determining the use condition of said memory chip**" (Lavallee, col. 12 lines 37-43, i.e., *"If the spare chip has already been used, the HAMT sends a report to the PCE so indicating. The HAMT hardware also indicate this condition in the current sparing vector and in response thereto, inhibits further sparing and further reporting of the "spare chip used" condition to the PCE (as related to the card being scrubbed)"* ).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to add the feature of determining the use condition of a memory chip, as taught by Lavallee, to the method of Butts so that the resultant method would determine the use condition of a memory chip and

configure file system accordingly. One would have been motivated to do so in order to in order to report the condition of the memory chip to the host system (PCE, processor controller element) (Lavallee, col. 12 lines 37-43).

As per claim 2, Butts in view of Lavallee teaches the limitation:

"**reading by a controller of the removable storage device, the amount of the memory chips installed in the removable storage device**" (Butts, Figure 2, note the memory chips (logic chips); Butts, col. 11 lines 60-64, i.e., *"logic chips laid out in a row-and-column 2-dimensional grid";* Butts, col. 12 lines 4-10, i.e., *" Depending on the number of logic chips and the numbers of pins on each one, a dimension and set of pin group sizes is chosen that will minimize the number of logic chips intervening between any two logic chips while providing enough interconnections between each directly neighboring pair of chips to allow for nets which span only those two chips"*) and "**obtaining information of storage capacity of each of said memory chip**" (*";* Butts, col. 12 lines 16-20, i.e. , *" In addition to partitioning the design into sub-networks which each fit with in a logic chip's logic capacity, the sub-networks should be placed with respect to each other so as to minimize the amount of interconnect required"* ).

As per claim 3, Butts in view of Lavallee teaches the limitation:

"**generating by aid host system, one or more disk descriptors for the removable storage device according to the information of the memory chips of said removable storage device**" ( Butts, col. 12 line 64 through col. 13

line 4, i.e., *"Issue these specifications in the form of I/O pin specifications and logic chip internal interconnections, along with the specifications of logic primitives, to the netlist file for each logic chip. Use the logic chip netlist conversion tool to generate configuration files for each logic chip, and combine them into* ***the final Realizer configuration file*** *for the input design"* ). Note that "the final Realize configuration file" maps to "disk descriptors" for the removable storage device according to the information of the memory chips" of the claim language.

As per claim 4, Butts in view of Lavallee teaches the limitation:

"**the number of the disk descriptors of the removable storage device is equal to the number of memory chips in the removable storage device**" (Butts, col. 12 line 64 through col. 13 line 4, i.e., *"Issue these specifications in the form of I/O pin specifications and logic chip internal interconnections, along with the specifications of logic primitives, to the netlist file for each logic chip. Use the logic chip netlist conversion tool to generate configuration files for each logic chip, and combine them into* ***the final Realizer configuration file*** *for the input design"* ).

As per claim 5, Butts in view of Lavallee teaches the limitation:

"**the memory chip of the removable storage device is divided into a plurality of partitions, the number of the disk descriptors of the removable storage device is equal to the number of the partitions**" ( Butts, col. 12 16-

16, i.e. *"Partition and place the logic primitives in the logic chips";* Butts, col. 12 line 64 through col. 13 line 4 as applied to claims 3 and 4 above).

As per claim 7, Butts in view of Lavallee teaches the limitation:

"**the installed memory chips are installed on the basis of the existing removable storage device**" (Butts, Figure 3, logic chips and Figure 38 ; Butts, col. 37 lines 38-44, i.e., *" FIG. 38 shows the USDM architecture. Devices are installed on the user-supplied device installation area, which can be an area of the USDM printed circuit board, a removable daughter card plugged into the USDM, or another such area connected via cable in the manner common in microprocessor emulator instruments*).

7. Claims 6 ,8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butts in view of Lavallee and further in view of Yasuda et al., (hereinafter "Yasuda", U.S. Patent Application Publication Number 2004/0010654).

As per claim 6, Butts in view of Lavallee teaches the limitations;

"**the memory chips include used memory chips and/or unused memory chips, the unused memory chips being original chips that have not been initialized or partitioned**" ( Lavallee, col. 12 lines 43-46, i.e., *" If the spare chip has not been used"* ), and **the step 1) further includes**:

"**determining whether the memory chips are used memory chips or unused memory chips, or include used and unused memory chips**"

(Lavallee, col. 12 lines 43-46, i.e., *" If the spare chip has not been used"* )

"**with respect to the unused memory chip, formatting the chips and establishing the file managing system**" ( Lavallee, col. 12 lines 46-47, i.e.,*" next, in step 636, the spare chip is initialized"* ).

Butts in view of Lavallee does not explicitly teach the limitation:

"if there are only used memory chips then, adopting the original file managing system thereof, **or** re-combining, modifying the file managing information and establishing new file managing system".

Yasuda teaches the limitation:

"(**if there are only used memory chips then), adopting the original file managing system thereof**" ( Yasuda, paragraph 0220, i.e., *"the virtualizing system on the new network storage accesses a local file system of either the existing network storage or the new network storage by using a standard file access protocol in accordance with a corresponding table indicating the relation between the network storage as a member and the unified identifier of the network storage which is managed by the virtualizing system. As a result, the* ***existing network storage*** *and the new network storage can be managed in a unified manner without setting special information in the existing network storage"* ).

Butts in view of Lavallee teaches used and unused memory chips. Yasuda teaches adopting existing file system of used storage devices by a network storage system by virtualization. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to add the feature of

adopting the existing file system of a used storage device, as taught by Yasuda, to the method of Butts in view of Lavallee so that the resultant method would adopt the original file system if there only used memory chips. One would have been motivated to do so in order to manage existing storages and new storages in a unified manner (Yasuda, paragraph 0220).

As per claim 8, Butts in view of Lavallee and further in view of Yasuda teaches the limitation:

"**determining the used memory chips include reading the logical "0" blocks of the memory chips, determining that the memory chips are used chips if no all logical "0" blocks are logical value "1", and determining that the memory chips are unused chips if all logical "0" blocks are logical value**" (Lavallee, col. 12 lines 43-46, i.e., *" If the spare chip has not been used* ).

As per claim 9, Butts in view of Lavallee and further in view of Yasuda teaches the limitation:

"**the types of the file managing system include file managing system supporting Windows and its updated version, or file managing system supporting UNIX or LINUX and their updated version, wherein the file managing system supporting Windows and the updated version includes but is not limited to: FAT12, VFAT, FAT16, FAT32, CDFS, NTFS; the file managing system supporting UNIX or LINUX and their updated version**

**includes but is not limited to: EXT2, EXT3, JFFS, NFS, RAMFS, HPFS, CRAMFS**" ( Yasuda paragraphs 0006 and 0058 ).

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Butts in view of Lavallee and further in view of Urabe (U.S. Patent Number 6182159).

As per claim 10, Butts in view of Lavallee does not explicitly teach the limitation: "reading designated address in the operation instruction, and transforming the designated address into physical address; and comparing the physical address with capacity of the memory chips, determining the corresponding memory chip, and finding corresponding storage block in the determined memory chip".

Urabe teaches the limitation:

"**reading designated address in the operation instruction, and transforming the designated address into physical address; and comparing the physical address with capacity of the memory chips, determining the corresponding memory chip, and finding corresponding storage block in the determined memory chip**" (Urabe, col. 4 lines 54-64, i.e., *"The memory controller 15 includes at least an address decoder for decoding a given address specified by a computer so as to enable one of the individual memory chips on the card 10'. The decoding of address is generally limited to an address range of the memory space defined by the plurality of the individual chips 11. In other words, based upon a specified type of memory and a specified extensive unique*

*address, a particular memory card is selected"*).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to add the feature of decoding a designated address into a physical address and determining a memory chip which has a capacity corresponding to the physical address, as taught by Urabe, to the method of Butts in view of Lavallee so that the resultant method would compare the physical address with capacity of the memory chips and determine the corresponding memory chip. One would have been motivated to do so in order to provide an efficient memory card management (Urabe, col. 2 lines 42-44).

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Butts in view of Lavallee and further in view of Urabe and further in view of Niles et al. (hereinafter "Niles", U.S. Patent Application Publication Number 2006/0236064).

As per claim 11, Butts in view of Lavallee and further in view of Urabe does not explicitly teach the limitation: "the removable storage device returns error information if the physical address exceeds the storage capacity of all memory chips of the storage device".

Niles teaches the limitation:

"**device returns error information if the physical address exceeds the storage capacity of all memory chips of the storage device**" ( Niles , paragraphs 0026-0029, i.e., *"Once the segment descriptor is allocated from the free list 2, a new segment descriptor is created by adding 100 to the starting*

*physical address field 12 and this is now the next free descriptor. Next, a check is performed to verify that the descriptor did not exceed its boundaries on its current physical drive. If the descriptor did not exceed its boundaries, nothing else is done until the descriptors are allocated. If the boundaries were exceeded, three things can happen: 1. It reached the virtual storage device and reached the end of its total capacity, no error is generated and an indicator is set to reflect this status. 2. It reached the end of its allocated disk area on its current physical drive and another physical drive is already available to continue its expansion, the fields in the free descriptor are updated to reflect the new disk. The fields include the starting physical address 12 and device ID 10 fields..3. It reached the end of its allocated disk area on its current physical drive and no drive is available to continue its expansion. Indicators are set to reflect this status and on the next segment allocation,* ***an error will most likely be generated****"*).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to add the feature of checking if a physical address would exceed the boundary of an allocated disk area and generating an error if it does, as taught by Niles, to the method of Butts in view of Lavallee and further in view of Urabe so that in the resultant method, removable storage device would return error information if the physical address exceeds the storage capacity of all memory chips of the storage device. One would have been motivated to do so in order to allow computer memory space, such as disk space, on demand rather than having the entire space pre-allocated (Niles paragraph 0002).

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Butts in view of Lavallee and further Hall et al. (Hereinafter "Hall", U.S. Patent Number 5939868).

As per claim 12, Butts in view of Lavallee does not explicitly teach the limitation: "the host system stops to supply removes power to the removable storage device or the controller of the removable storage device when replacing the memory chips for the removable storage device".

Hall teaches "removing power to memory chips when replacing the memory chips" ( Hall, col. 6 lines 42-44, i.e, *"Typically, chips are changed on a circuit board only after power to the board is turned off"* ).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to add the feature of turning off the power supply to memory chips when replacing the memory chips, as taught by Hall, to the method of Butts in view of Lavallee so that the resultant method would remove power to the removable storage device when replacing the memory chips for the removable storage device. One would have been motivated to so in order to avoid electrocution or damage to memory chips.

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Butts in view of Lavallee and further Moore et al. (Hereinafter "Moore", U.S. Patent Application Publication Number 2005/0223243).

As per claim 13, Butts in view of Lavallee does not explicitly teach the

limitation: “setting data encryption area in the memory chips, and performing encryption or decryption to the stored data by the controller of the removable storage device”.

Moore teaches the limitation:

“**setting data encryption area in the memory chips, and performing encryption or decryption to the stored data by the controller of the removable storage device**” ( Moore, Abstract, paragraphs 0005, 0026, and 0027 ).

At the time the invention was made it would have been obvious to a person of ordinary skill in the art to add the feature of setting data encryption area on a memory and performing data encryption/decryption, as taught by Moore, to the method of Butts in view of Lavallee so that the resultant method would set data encryption area in the memory chips and perform encryption/decryption to the stored data. One would have been motivated to do so in order to prevent unauthorized use or copying of program code stored on a memory device (Moore, paragraph 0026).

## ***Contact Information***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DENNIS MYINT whose telephone number is (571)272-5629. The examiner can normally be reached on 8:30AM-5:30PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on (571) 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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